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Silicon Island Insights

Beyond the Chip: Key Forces Reshaping the Global Semiconductor Industry

Top News

Research & Analysis

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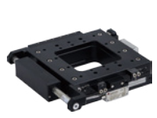
PBA Systems Hot Products

DX F Series Ironless Linear Motor	PIXB Series Ironcore Linear Motor	CVC Series Circular Voice Coil Motor	ARC Series Ironless Arc Motor	PDDR/PDDRB Series Direct Drive Rotary Motor
				
PLA Series **Linear Actuator**	**PZA H Positioing** **Actuator**	**XYZ Module with** **Dual Carriage**	**High Precision Stages**	**PABG1000 Air Bearing** **Nano Precision Gantry**
				

High Precision Stages

High Speed High Precision Dual Gantry Stage	PABG 2000 XYZ Co-Planar Theta Gantry	PFG 6000 Thermo-Compression Bonding Gantry	Planar XY Clear Aperture High Precision Stage
			

SEMICON TAIWAN

Meet-the-Expert Stage
#Q6252

TOPIC

Next-Generation Precision Motion Platform Technologies for Semiconductor Advanced Packaging & CPO in the AI Era

TIME 2026/9/04

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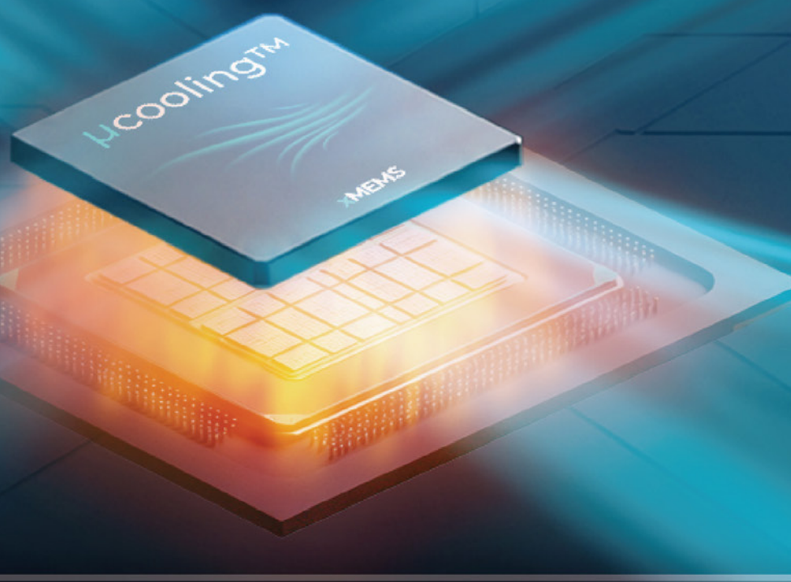

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SEMICON Taiwan reaches record scale, forging new opportunities across the full value chain in the AI era

Monica Chen, Taipei

SEMICON Taiwan 2026 will take place from September 2 to 4 under the theme "Transform Tomorrow—Building the Future Together." The event is expected to bring together more than 1,300 exhibitors and 4,300 booths, setting records in both categories, and is anticipated to attract more than 100,000 industry professionals from 65 countries. Continuing its "International Semiconductor Week" format, the event will kick off with a series of international forums on August 31, while its exhibition footprint will also expand further, reflecting the continued growth of the global semiconductor ecosystem driven by AI.

SEMI said the rapid development of AI, high-performance computing (HPC), and emerging applications is extending competition in the semiconductor industry beyond advanced process technologies to advanced packaging, smart manufacturing, quantum technology, and system integration. SEMICON Taiwan 2026 will broaden its focus from individual process technologies to ecosystem-wide collaboration, highlighting a new strategy for Taiwan's semiconductor supply chain as it builds on its manufacturing strengths to compete across the full value chain.

According to SEMI statistics, the global semiconductor manufacturing equipment market reached US$135.1 billion in 2025, a year-over-year increase of 15%, and is projected to grow further to US$145 billion in 2026. Meanwhile, global investments in 300mm wafer fab equipment are expected to exceed US$150 billion for the first time in 2027, indicating that demand for AI chips continues to drive investment in advanced processes, memory, advanced packaging, and the broader supply chain.

SEMI said no single company can independently advance all technologies required in the AI era. Only through cross-disciplinary ecosystem collaboration can the industry capture the next wave of growth opportunities. The 2026 exhibition will therefore focus on several core areas, including AI, smart manufacturing, quantum technology, advanced packaging, startups, and talent development.

In response to technological advances across the industry, SEMICON Taiwan 2026 will introduce the Quantum Technology Zone and Smart Fab Zone for the first time, while adding a dedicated Chiplet Pavilion to the Packaging Technology Area, constituting three of the exhibition's major new highlights.

The Quantum Technology Zone will showcase different technological pathways, including superconducting systems, trapped-ion systems, and quantum annealing. It will connect government agencies, academic and research institutions, and international quantum-computing companies to accelerate the development of Taiwan's quantum technology ecosystem. The Smart Fab Zone will focus on AI, autonomous decision-making, digital twins, automated material handling systems (AMHS), and collaborative and humanoid robots, demonstrating next-generation production models as wafer fabs progress from automation toward intelligent and autonomous operations.

In advanced packaging, the Packaging Technology Area will encompass four major themes: 3D IC advanced packaging, fan-out panel-level packaging (FOPLP), semiconductor packaging, and chiplets. It will bring together nearly 300 domestic and international companies, including Lam Research, Hanwha Semitech, and Resonac, with a focus on key technologies such as hybrid bonding, electroplating, panel-level processing, and heterogeneous integration.

SEMI further explained that as applications such as AI servers, data centers, autonomous

In the face of concerns of an AI bubble, the fever pitch at SEMICON Taiwan 2026 may tell the real story. Credit: Michael Lee

driving, and 6G develop rapidly, chiplet architecture is increasingly becoming an important design approach for improving computing performance and reducing costs. Heterogeneous integration and advanced packaging can overcome the performance, size, and yield limitations of individual chips, making chiplets a critical technology in the evolution of AI chips.

Smart manufacturing, meanwhile, is the fastest-growing exhibition category in 2026. SEMI said the Smart Manufacturing Pavilion has not only grown by 20% from 2025 to become the event's largest exhibition area, but it will also bring together nearly 350 companies, including Advantech, Delta Electronics, OMRON, Siemens, and Techman Robot. They will showcase solutions for AI visual inspection, smart factories, automation control, the industrial Internet of Things (IoT), and edge AI.

Magic Pao, vice president of Advantech's Edge Server Group, pointed out that AI is gradually moving from the cloud to the factory floor. AI-powered decision-making systems can enable production lines to achieve 100% autonomous route planning, improve utilization rates by 15% to 20%, and greatly reduce decision-making time. This demonstrates that the adoption of AI in manufacturing has progressed from proof-of-concept to large-scale deployment.

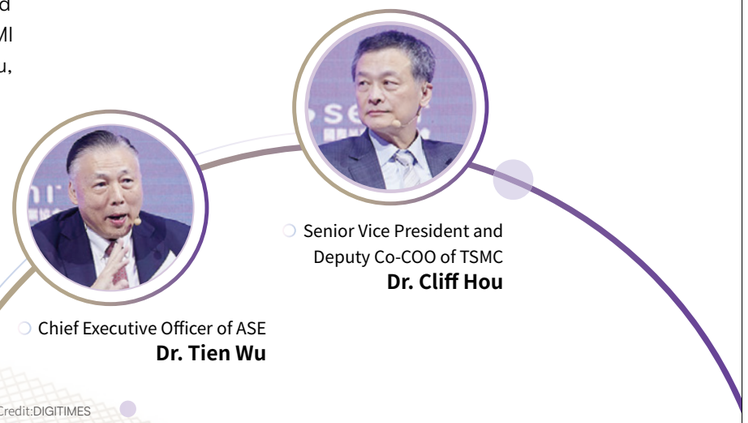
Furthermore, SEMICON Taiwan 2026 will continue strengthening its three main pillars of AI semiconductors, startups, and talent

development. The AI Technology Zone will also present the complete ecosystem for AI chips, from advanced processes and application-specific integrated circuit (ASIC) design to edge AI applications. The Silicon Startups Zone, jointly promoted by SEMI and Taiwan's National Science and Technology Council (NSTC), will incorporate teams from the IC Taiwan Grand Challenge to help semiconductor startups from around the world connect with Taiwan's supply chain and investors, accelerating the commercialization of their technologies.

The event will also hold more than 22 professional forums covering advanced packaging, memory, geopolitics, sustainability, cybersecurity, talent, and other subjects. The CEO Summit & Ecosystem Executive Summit on September 2 is set to be a particular highlight. Speakers will include Rani Borkar, president of Azure Hardware Systems and Infrastructure at Microsoft; Asad Khamisy, senior vice president and general manager at Broadcom; Alexander Gorski, chief operations officer at Infineon Technologies; Michael Kagan, chief technology officer at NVIDIA; and senior global technology and semiconductor executives from Micron Technology and other companies. They will explore new directions for collaboration across semiconductors, cloud computing, and the broader technology ecosystem in the AI era.

The closing fireside chat will be co-moderated by Tien Wu, CEO of ASE and chair of the SEMI International Board of Directors, and Cliff Hou, TSMC's deputy co-chief operating officer and chairman of the Taiwan Semiconductor Industry Association (TSIA). They will be joined on stage by MediaTek vice chairman and CEO Rick Tsai and Unimicron chairman Shan-Chieh Chien. Drawing on perspectives spanning IC design, wafer manufacturing, advanced packaging, substrates, and system integration, the participants will discuss trust in technology during the AI era, global supply-chain collaboration, and the direction of semiconductor industry development over the next decade.

The most closely watched pre-show event will be the Silicon Photonics Global Summit, which will bring together industry leaders from across the global silicon photonics ecosystem, encompassing system architecture, optical interconnect technology, advanced manufacturing, and other fields. Participants will discuss how silicon photonics technology can steadily progress from innovative research and development to large-scale mass production and commercial deployment. Speakers will include senior executives from TSMC, ASE, UMC, ficonTEC, Cisco, Lightmatter, Lumentum, Marvell, Lam Research, and other major companies.



Senior Vice President and Deputy Co-COO of TSMC
Dr. Cliff Hou

Chief Executive Officer of ASE
Dr. Tien Wu

Credit:DIGITIMES

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Interview

Innovative Solutions for Fabricating High-Performance AI Multichip Packaging Using Glass Substrates

Interested in knowing how to solve the microcrack problem in through-glass via (TGV) fabrication? Interested in knowing how to supply 1,000 Watts, 1 Volt and 1,000 Amperes electricity to semiconductor IC chips in an AI multichip package? Interested in knowing how to increase the glass panel size for manufacturing AI multichip packages? If so, visit iCometrue® at Booth M0957, Hall 1, 4F, Taipei Nangang Exhibition Center during SEMICON Taiwan 2026!

Benefiting from their excellent thermal, mechanical, and electrical properties, glass substrates have emerged as a promising platform for large-size, high-performance AI multichip packages. At SEMICON Taiwan 2025 last year, iCometrue® exhibited the Through-Polymer-Via (TPV) Connector, a novel technology that provides vertical interconnection in Glass Cores for use in Glass Interposers and BGA substrates to solve the microcrack problem in glass substrates caused by TGV fabrication.

At SEMICON Taiwan 2026 this year, iCometrue® plans to exhibit solutions for delivering over 1,000 W and over 200 A of power supply to the high-performance AI multichip package. The solutions include:

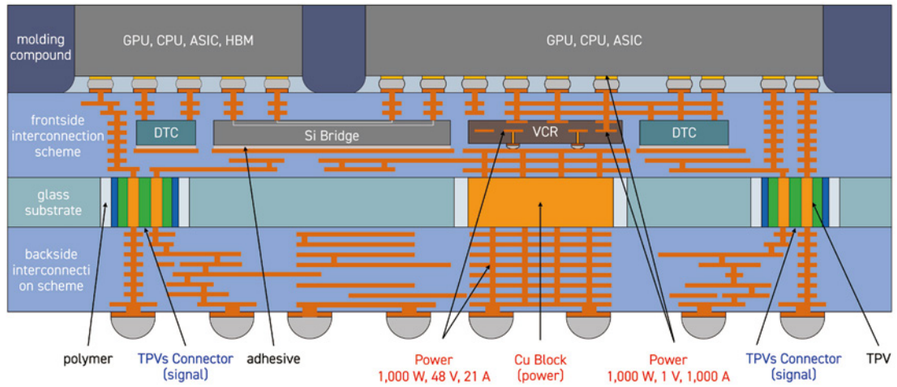
(1) Embedding Cu Blocks in Glass Substrates for Power/Ground Delivery

Cu blocks are used to replace TPVs/TGVs for power/ground delivery. This approach significantly reduces the number of TPVs/TGVs originally used for power/ground delivery through the glass substrate by 80%, thereby lowering fabrication complexity, improving manufacturing yield, and reducing manufacturing costs.

A current high-performance AI multichip package, comprising GPU chips and HBM modules, has more than 10,000 I/Os for power, ground, signal, and clock distribution, which requires more than 10,000 TGVs/TPVs in the glass substrate. 80% of these TGVs/TPVs in the glass substrate are used for power/ground delivery. Using Cu blocks to replace TPVs/TGVs for power/ground delivery results in an 80% reduction in the number of TPVs/TGVs, thereby lowering fabrication complexity, improving manufacturing yield, and reducing manufacturing costs. Nowadays high-performance semiconductor IC chips in AI multichip packages typically require more than 1,000 W of power. Since power (P) is given by P = I x V, a 1 V operation voltage of semiconductor IC chips corresponds to a current over 1,000 A.

As shown in Fig. 1, the embedded Cu blocks provide the power/ground voltage and current paths that would otherwise require a large number of TPVs or TGVs in the glass substrate. The remaining TPVs/TGVs (approximately 20%) are reserved for signal and clock transmission. Consequently, the embedded Cu blocks significantly reduce the number of TPVs/TGVs in the glass substrate.

The formation of embedded Cu blocks in glass substrates is achieved by inserting Cu blocks into pre-formed large holes in the glass substrate. This process is similar to the TPV Connector embedding process in glass substrates previously disclosed at SEMICON Taiwan 2025.



Innovations in Fig. 1:

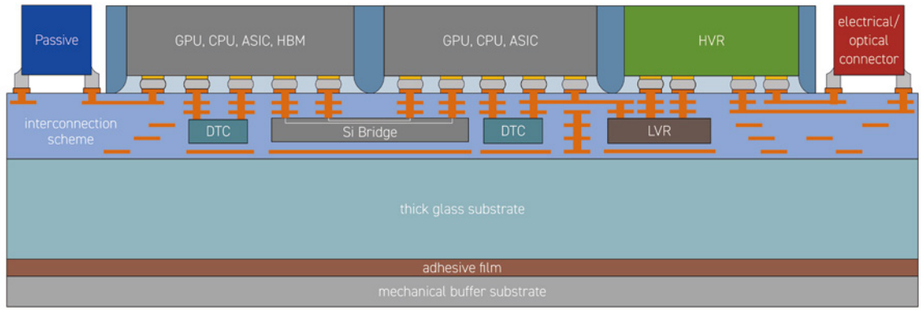
- Embedding Cu blocks in glass substrates for power/ground delivery.
- Packaging High Voltage Converter/Regulator (HVCR) chips in the AI multichip package, allowing high-voltage power supply input to the package and reducing power supply voltage within the package.
- Embedding Si bridges, deep-trench decoupling capacitors (DTCs), and Low Voltage Converter/Regulator (LVCR) chips in the frontside interconnection scheme over the glass substrate.

(2) Packaging Voltage Converter/Regulator (VCR) chips in AI Multichip Packages

The VCR chips are packaged vertically under and close to the GPU chip within the AI multichip package. The embedded VCR chips convert the 1,000 W, 48 V, 21 A power supply from external circuits to 1,000 W, 1 V, 1,000 A for the GPU chip. As shown in Fig. 1, copper blocks provide a low resistance power delivery system from external circuits to the embedded VCR chips, and resulting in reduction of the heat generation.

(3) Embedding Si Bridges, DTCs, and VCR chips in the Frontside Interconnection Scheme Over the Glass Substrate

At SEMICON Taiwan 2025, iCometrue® demonstrated that Si bridges and DTCs are embedded in large holes within the glass substrate. Here in Fig. 1, iCometrue® shows that Si bridges, DTCs, and VCR chips are instead embedded in the frontside interconnection scheme over the glass substrate, while the TPV connectors and copper blocks are embedded in large holes in the glass substrate. This approach further simplifies the fabrication of the AI multichip package using a glass substrate.



Innovations in Fig. 2:

- Installing electrical/optical connectors at the edges of the Al multichip package, replacing solder bumps for interfacing with external

(4) Installing Electrical/Optical Connectors at the Edges of the Al Multichip Package

When glass substrates are used for multichip packaging, power and signals are usually input and output via the solder balls on the bottom of the multichip package through the backside interconnection (under the glass substrate), TPVs/TGVs (in the glass substrate), and the frontside interconnection (over the glass substrate) to the semiconductor chips. As discussed above, the fabrication of TPVs/TGVs is one of the major challenges in glass-substrate technology. To solve this problem, iCometrue® has introduced an innovative architecture that enables a large-size System-on-Panel (SOP) multichip package using a thick glass substrate without TPVs/TGVs.

As shown in Fig. 2, power and signals are delivered through electrical and/or optical connectors located at the edges of the multichip package rather than through solder balls on the bottom of the package. The glass substrate is used as a panel-level fabrication platform and remains in the final package to provide mechanical support. An interconnection scheme (metal line and polymer) is built on the glass substrate, with electronic components such as interconnection bridges, integrated passive devices (IPDs), and VCR chips embedded within it. Semiconductor chips (CPU, GPU, ASIC, HBM) are then flip-chip bonded onto the interconnection scheme above the glass substrate. Electrical and/or optical connectors, together with passive components, are mounted on the top surface of the interconnection scheme using surface-mount technology (SMT).

Because power and signals are supplied by the edge connectors instead of bottom solder balls, signal transmission and power distribution from the edge connectors to semiconductor chips are through the interconnection scheme. Consequently, no TPVs or TGVs are required in the glass substrate, enabling large-size System-on-Panel (SOP) packages. Further, since no TPVs or TGVs are required, a thicker glass substrate can be used, which greatly reduces the bending of the glass panel. Thereby, the size of the glass panel used in the fabrication can be greatly increased.

More than Moore: The Use of Glass Substrates for Multichip Packaging

iCometrue® is pioneering a new era of advanced multichip packaging by introducing glass substrates with embedded TPV Connectors and Cu blocks, providing a practical and scalable alternative to conventional TGV-based processes. Further, embedding Si bridges, DTCs, and VCR chips in the frontside interconnection scheme over the glass substrate simplifies the fabrication of the Al multichip package. Combined with the TPV/TGV-free thick glass substrate architecture for System-on-Panel (SOP) packaging, these technologies establish a foundation for the next generation of multichip integration, extending Moore's Law into the era of glass-based system packaging and accelerating the advancement of high-performance computing (HPC) and AI applications.

800VDC becomes essential for AI data centres, with GaN critical to voltage conversion

DIGITIMES Intelligence, C. Y. Yao

DIGITIMES notes that Rubin Ultra GPUs are expected to enter mass production in 2027, when Power Sidecar cabinets will supply 800VDC directly to compute racks. Within the compute racks, power conversion will extend beyond the existing 800VDC-to-54VDC architecture to 12VDC and 6VDC rails, now key development targets for power semiconductor suppliers. This shift will make gallium nitride (GaN) devices increasingly critical and could allow them to replace conventional silicon MOSFETs in secondary-side circuits.

Current GB200 and GB300 racks still largely require conventional 48VDC to 54VDC inputs. Vera Rubin racks, expected to gain market attention in 2026, are also likely to retain a 54VDC design to remain compatible with existing power infrastructure. Native 800VDC input is expected to arrive with Rubin Ultra, better known as the NVL 144 Kyber compute rack.

DIGITIMES believes Nvidia introduced the 800VDC concept in 2025 to address the rising power demands of next-generation GPUs, prompting its broader ecosystem to develop solutions around the new architecture. Public disclosures and product plans from semiconductor suppliers remained relatively vague at the time, but by 2026, Taiwan-based suppliers had accelerated preparations and Nvidia's product roadmap through 2028 had become clearer. Major power semiconductor vendors consequently began aligning their strategies with AC/DC Power Sidecar cabinets and rack-level voltage conversion designs targeted for 2027 and 2028, particularly for the Rubin Ultra and Feynman GPU platforms.

Advanced process roadmap for TSMC, Intel, and Samsung Electronics

NVIDIA GPU products	Vera Rubin	Rubin Ultra	Feynman
Mass-production timing	2026	2H 2027	2028
Maximum scale-up configuration	NVL72	NVL144	NVL1152
Power per compute rack	220kW	600kW	1MW
Power-supply design	No standalone power-supply rack required; the compute rack incorporates a power shelf delivering 54 VDC	· A standalone Power Sidecar rack supplies 800 VDC · Compute rack integrates an 800 VDC-to-54 VDC power shelf · Ultimate target: 800 VDC-to-54 VDC power delivery board (PDB)	· Power Sidecar racks become the mainstream power-supply architecture · Solid-state transformers directly supply 800 VDC, entering low-volume production
Evolution of DC power-delivery architecture	· 54 V-12 V · 12 V-6 V · 6 V-0.x V	· 800 V-54 V, 12 V, 6 V · 12 V-6 V · 6 V-0.x V	· 800 V-54 V, 6 V · 54 V-12 V · 6 V-0.x V

Source: Vendors, DIGITIMES compilation, 2026.8

Power semiconductor vendors target 2027 as next-gen GPUs drive higher power demand

Leading global power semiconductor suppliers can broadly be divided into three groups: those offering both silicon carbide (SiC) and GaN devices, those focused solely on GaN, and those focused solely on SiC. Infineon, STMicroelectronics, Navitas and ROHM offer both technologies, while Texas Instruments and Renesas focus on GaN. Wolfspeed, which recently emerged from bankruptcy protection, remains primarily focused on SiC.

As AI servers enter the Vera Rubin generation, rising compute-rack power requirements are accelerating demand for standalone Power Sidecar cabinets. Under this architecture, the Power Sidecar converts 480VAC into 800VDC, while the compute rack performs successive voltage step-downs from 800VDC or 54VDC until stable DC power can be delivered to the GPUs and ASICs responsible for computation.

Both 54VDC- and 800VDC-based compute racks require step-down conversion. DIGITIMES notes that since 2026, power semiconductor vendors have increasingly highlighted 800VDC-to-12VDC and 800VDC-to-6VDC solutions, shifting attention away from 800VDC-to-54VDC conversion. Power conversion and transmission circuits must be designed around the performance requirements of GPUs and ASICs. To support rack deployments in 2026 and 2027, the relevant chip specifications therefore had to be finalised in 2025, allowing OEMs and ODMs to move the systems into mass production the following year.

Key 2026 power semiconductor developments in the Nvidia ecosystemElectronics

	Timing	Key release points
STMicroelectronics	2026.03	Demonstrated power distribution board (PDB) architectures for 800 VDC-to-12 VDC and 800 VDC-to-6 VDC at GTC 2026
Texas Instruments	2026.03	GTC 2026 demo · 800 V hot-swap controller · 800 VDC-to-6 VDC integrated bus converter (IBC) · 6 V to <1 V multiphase buck converter · 800 V-to-12 V DC/DC bus converter
onsemi	2026.05	Broad portfolio of MOSFETs, GaN, SiC power devices, and SiC JFETs supports the flexible mix-and-match architecture at the core of the MGX ecosystem
Innoscience	2026.05	Advancing all-GaN power conversion technology
Infineon	2026.05	· Power management solutions support the MGX architecture and 800 VDC power architecture · Can convert 800 VDC to 50 V, 12 V, or as low as 6 VDC
Analog Devices	2026.05	· To address 800 VDC hot-swap circuit design, it provides fast, accurate protection and advanced telemetry for system optimization and predictive maintenance · 800 VDC-to-6 VDC solution already available
Navitas	2026.06	· Demonstrated an 800 VDC-to-6 VDC power distribution board (PDB) at COMPUTEX 2026 · SiC devices introduced in solid-state transformers (SSTs) and power supply units (PSUs)
EPC	2026.06	· Released GaN power devices to meet 6 kW 800 VDC-to-12.5 VDC design requirements

Source: Vendors, DIGITIMES compilation, 2026.8

800VDC conversion moves to lower voltages as GaN becomes indispensable

System architectures that begin voltage conversion from 800VDC generally use intermediate bus converters (IBCs), power distribution boards (PDBs) or Power Shelf-like designs. Industry definitions separating IBCs from PDBs remain relatively fluid on the 800VDC step-down side, while 12VDC and 6VDC conversion modules are generally classified as medium- to low-voltage IBCs.

Module and system dimensions vary according to power rating. In the IBC market, a quarter-brick module currently supports about 3kW, while a half-brick module can handle roughly 6kW.

Since NVIDIA launched the 800VDC power architecture concept for AI servers in 2025, there has been little further update on 800VDC in 2026. However, as Vera Rubin moves toward mass production, a number of power semiconductor vendors have begun releasing solutions related to 800VDC-to-12VDC or 800VDC-to-6VDC.

DIGITIMES observes that primary-side power semiconductor solutions are largely based on GaN devices, while the secondary side uses silicon MOSFETs. However, only vendors such as onsemi, Analog Devices (ADI), and Innoscience have not further specified the mechanical design and power levels for the corresponding 800VDC-to-12VDC or 800VDC-to-6VDC solutions. Innoscience has also announced 40V and 15V GaN products for 800VDC-to-12VDC and 6VDC architectures, respectively. DIGITIMES believes this suggests Innoscience intends to introduce GaN devices on the secondary side to replace conventional silicon MOSFETs.

Technology continues to advance; secondary-side design is already considering GaN replacement

As is well known, SiC and GaN devices have overlapped in some applications in the past. But as technology has advanced, SiC voltage-withstand capability has gradually improved, while GaN has relied on high switching frequency and the ability to integrate gate-drive components. As AI server power continues to rise and system volume remains constrained, GaN devices clearly have room to demonstrate their strengths. Looking only at the 800VDC step-down design, there has long been debate over which is stronger, SiC or GaN. SiC devices have higher voltage-withstand capability and can complete primary-side functions with a single device, whereas GaN still requires a series configuration to handle the load. However, GaN's high-frequency characteristics do provide advantages in high-power-density power designs.

Meanwhile, as GaN devices continue to evolve, some vendors are considering introducing them on the secondary side as well. The main reason is that the conduction-loss performance of new-generation GaN devices is already better than that of conventional silicon MOSFETs. In an 800VDC-to-6VDC circuit, where power delivery is relatively close to the GPU, strengthening the high-current point of load (POL) (point of load) conversion stage with low-voltage GaN devices would help downstream high-current POL regulators deliver ultra-low voltage to the GPU efficiently while maintaining fast transient response. In addition, if the pinout remains compatible with silicon MOSFETs, adoption becomes easier and supports broader improvements in power-design efficiency.

2026 AI server rack 800 VDC step-down designs

	800VDC-12VDC		800VDC-6VDC	
	Primary and secondary sides Power device category	Mechanical design - Power level	Primary and secondary sides Power device category	Mechanical design - Power level
Infineon	GaN+Si	IBC-6kW PDB-12kW	GaN+Si	
ST life.augmented	GaN+Si	PDB-6kW	GaN+Si	PDB-20kW
Texas Instruments	GaN+Si	PDB-12kW	GaN+Si	PDB-20kW
Navitas	GaN+Si	PDB – power not disclosed	GaN+Si	PDB-20kW
Renesas	GaN+Si		GaN+Si	IBC-20kW
EPC	GaN+GaN	Mechanical design not disclosed – 6 kW	GaN+GaN	

Source: Vendors, DIGITIMES compilation, 2026.8

Conclusion

What's clear is that once the Rubin Ultra GPU enters mass production in 2027, Power Sidecar cabinets will supply 800VDC to compute racks. At the same time, within compute-rack step-down design, beyond the existing 800VDC-to-54VDC conversion, 12VDC and 6VDC are also major priorities for most power semiconductor vendors. GaN devices will therefore become indispensable, with the potential to replace conventional silicon MOSFETs in secondary-side circuits as well.

DIGITIMES believes that the development path for the power infrastructure required by AI data centers, as well as the power devices needed for compute racks, is already broadly clear for the next few years after 2026. The market will be shaped by how vendors balance total device cost, mechanical design, power density, and energy efficiency. That said, as the 800VDC landscape becomes clearer and even standardized, vendor supply capability, along with original equipment manufacturer (OEM) and original design manufacturer (ODM) system design and bargaining power, should become another key issue in 2027 and 2028.

Interview

Manz Asia Omni series pioneered ECD and wet-process platform, creating a comprehensive portfolio of panel-level packaging systems for 310, 510, and 700mm substrates

Rapid evolution of High-Performance Computing (HPC) and artificial intelligence chips for Hyperscalers and tech giants continue pushing large sized silicon demands. As a core element of semiconductor value creation, advanced packaging technology is scaling the stacking of more computing cores, more high-bandwidth memory, as well as the adoption of modular chiplet integration to overcome physical boundaries. Leading semiconductor manufacturers are expanding package dimensions to unprecedented footprints, currently reaching sizes of 100, 120, with projections moving beyond 180 mm to support large-format AI-driven advanced packages.

The semiconductor industry is responding and shifting toward solutions that combine large-scale mass production with large-format packaging capabilities. Square sized substrates offer a distinct area utilization advantage to accommodate more large-form-factor chips simultaneously by moving away from round wafers to large rectangular panels. This is improving cost efficiency and addressing the challenges of thermal warpage and high-density interconnects associated with massive AI packages.

Glass substrates are emerging as a key technology for advancing panel-level packaging from pilot experiments to active equipment qualification and commercialization verification. Consequently, Redistribution Layer (RDL) wet process and ECD equipment has become a critical driver of this transition and a key step in glass substrate manu-facturing. Key production tools including Electrochemical Deposition (ECD), cleaning, developing, etching, and stripping are not only vital to glass core substrate manufacturing, but also central to achieving high yields and mass production capabilities in advanced packaging technologies such as fan-out panel-level packaging (FOPLP) and Chip-on-Panel-on-Substrate (CoPoS). The wet processing equipment has garnered significant market attention.

Omni production platform supports cross-sized substrates in 310, 510 and 700mm panel

Manz Asia, has successfully delivered Omni 310 system, which is the world's first 310mm × 310mm ECD wet chemistry system in early 2026. The system uses an electrochemical deposition module as its core, combining wet processing tools including cleaning, developing, plating, etching, stripping, and dual mechanisms support for both spin and spray operation. This new platform addresses the adaption to varying rectangular substrates.

At SEMICON Taiwan 2026, Manz Asia expanded its portfolio with the launch of the cross-sized Omni series production systems. Engineered for varying panel dimensions, packaging architectures, and strict process requirements, this series feature the Omni 310, Omni 510, and Omni 700 to deliver optimized panel-level packaging (PLP) solutions across 310mm, 510mm, and 700mm panel sizes to meet the requirements of advanced PLP technology roadmaps including FOPLP, CoPoS, and Glass core TGV manufacturing.

Take early-move positioning for Glass Core substrate aiming to tackle Through-Glass Via challenges

Rapid advancements in CoPoS are driving the shift from organic substrates to Glass Core, with TGV metallization, seed-layer formation, and copper via filling emerging as key process challenges. The Omni Series RDL platform integrates glass surface modification, cleaning, electroless copper plating, and electroplating to enhance copper adhesion and enable reliable TGV metallization and filling. Major Benefits of Omni series include,

High performance ECD technology: The system offers excellent capabilities for filling high-aspect-ratio through-vias. When combined with an optimized seed layer and specialized plating chemistry, this process enables void-free via filling, delivering a highly stable and critical solution for electroplating on glass carrier substrates.

High-precision glass etching technology: Featuring robust glass micro-machining capabilities, this technology supports the processing of 0.4 mm glass substrates and the creation of 20 µm micro-vias. It offers TGV process capabilities with aspect ratios of up to 1:20, providing a critical advantage for achieving deep, fine-featured vias. Therefore, the system addresses the challenges of high-density TGV designs and marks a milestone in establishing a mass-production platform for next-generation packaging architectures.

Empowering Heterogeneous Integration with advanced RDL for High-Precision Multi-Layer Interconnection

With 40 years of in-house R&D expertise in RDL processing, Manz Asia has developed extensive expertise across PCB, IC substrate, display panel, and semiconductor packaging applications, and is now building strong collaborations with global IDM and OSAT clients. By helping customers accelerate key process iterations and transition smoothly to mass production, Manz Asia plays an active role in the global RDL processing and panel-level packaging supply chain.

Designed for next-generation advanced packaging technologies like CoPoS, FOPLP, and Glass Core TGV, the debut of the Omni series production systems helps customers accelerate their transition from R&D validation to mass production. To learn more about Manz Asia production systems and product offerings, please visit the booth M1248, 4th Floor, Hall 1, Nangang Exhibition Center at SEMICON Taiwan 2026. You can also view detail product information on the official website at www.manz.com.tw

Is the cloud AI investment boom overheating? Three key pavilions at SEMICON Taiwan 2026 will reveal the truth

Jay Liu, Taipei

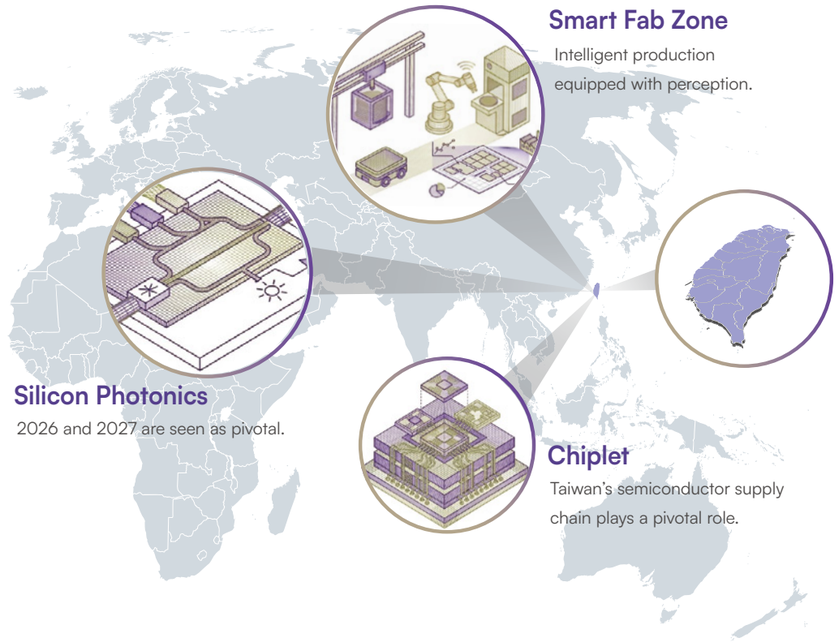
The scale of capital expenditure for cloud AI continues to redefine market expectations, but doubts about whether this wave of investment is overheating and potentially heading toward a bubble have surfaced along with it. SEMICON Taiwan, scheduled for September 2026, may provide the best opportunity to put that concern to the test.

Looking at the scale of this year's event, the exhibition is expected to bring together over 1,300 exhibitors and 4,300 booths, both record highs. For the first time, it will also extend to additional venues, including the Grand Hilai Taipei and Grande Luxe Banquet. According to SEMI's estimates, global semiconductor equipment investment is projected to grow further to US$145 billion in 2026. Judging by the momentum of equipment investment, the market has yet to show signs of cooling down, and the risk of a bubble remains manageable.

Meanwhile, SEMI's global chief marketing officer and president for Taiwan Terry Tsao previously addressed the possibility of an AI bubble. He pointed out that the essence of the dot-com bubble was "overcapacity," where demand could not keep pace with the frenzied infrastructure buildout. However, the current AI landscape is the exact opposite, with the supply of computing power and technical specifications constantly racing to catch up with ever-rising demand.

At SEMICON Taiwan 2026, three key pavilions can serve as important barometers. All three center on critical technological bottlenecks for the coming AI era. These technologies can no longer merely remain at the conceptual level; the question now is “how to put them into practice”.

Therefore, the intensity of discussion surrounding the following technologies will reveal whether cloud AI semiconductors are still struggling to meet demand in terms of both production scale and technological capability.



The first indicator is silicon photonics. The years 2026 and 2027 are seen as pivotal for the commercial deployment of co-packaged optics (CPO). TSMC is moving its COUPE platform toward volume production, NVIDIA has positioned CPO as a necessary path for network bandwidth expansion, and Broadcom has begun shipping CPO-enabled switch chips to early customers.

The 2026 Silicon Photonics Global Summit is bound to center on practical aspects such as mass production and validation, proving that silicon photonics is no longer just a buzzword, but a substantive demand.

The second indicator is the Chiplet Pavilion, which will debut within the Packaging Technology Area. Through advanced packaging and heterogeneous integration, the chiplet architecture modularizes bare dies from different process nodes and integrates them into a single package, addressing real bottlenecks involving AI chip design complexity, performance, and cost.

Taiwan's semiconductor supply chain—including packaging and testing providers, substrate makers, and equipment vendors—is playing an increasingly critical role in the chiplet field, indirectly proving that AI demand is not merely hot air.

The third indicator is the Smart Fab Zone. Semiconductor fabs are gradually transitioning from automation toward intelligent production systems equipped with perception and decision-making capabilities.

SEMICON Taiwan 2026 is expected to showcase a concentration of technology applications such as collaborative robots, humanoid robots, automated material handling systems (AMHS), and digital twins. Their prominence reflects the simultaneous pressures on the semiconductor industry to expand capacity and cope with labor shortages, making smart manufacturing a core issue for meeting the massive demand for cloud AI.

Interview

Keywave Technology innovative radar sensors spark a smart sensing revolution

Ian Sward, Product Director, presents Keywave's microwave radar sensor product offerings and strategies

Keywave Technology is a fabless semiconductor company founded in December 2022 that specializes in radio frequency (RF) integrated circuit (IC) design and advanced radar sensing solutions. Capitalizing on the explosive growth of Edge AI and opportunities for technological innovation, the company builds ultra-low-power microwave radar chips, modules and spatial sensing devices to track multiple targets with centimeter-level precision spatial positioning applications.

Keywave Technology currently business focuses primarily on the UK market, where it has achieved significant success in projects spanning lighting, energy-saving systems, HVAC optimization, and smart applications involving precise occupancy tracking, smart environmental sensing and human-machine interaction.

Jenny Cheng, founder and CEO of Keywave, established an office in Zhubei as early as 2023 and marked a strategic expansion into Taiwan's core semiconductor and electronics ecosystem. Recognized strong growth of Taiwan's electronics manufacturing and semiconductor market, she formally launched an "Asia Business Division" team in 2026 with over 20 members.

Following collaboration and engagement with major Taiwanese electronics manufacturing, and OEM/ODMs, Keywave has developed two radar sensor product lines, operating at 5.8 GHz and 24 GHz targeting markets such as AI robotics, smart spaces, smart buildings, automation, and edge AI sensing. Through proof-of-concept (PoC) initiatives and product design, the Keywave R&D team has focused on applications requiring high-precision spatial sensing and trajectory tracking. These innovative products, characterized by high accuracy, rapid sensing capabilities, energy efficiency, and cost-effectiveness. Now these solutions are being officially introduced to Taiwan's industrial internet of things (IoT) and automation sector, paving the way for new business opportunities.

MP Kan, VP of Technology and CTO at Keywave, outlined the shortcomings of traditional microwave radar and infrared (PIR) sensing technologies. Benchmarked against radar devices from leading global analog integrated circuits (ICs) manufacturers, he identified the primary drawbacks of these existing solutions: false detections leading to unintended activations, a technical inability to detect motionless objects or resting human bodies, and issues regarding high costs and excessive power consumption.

In contrast, Keywave KW007, the compact 5.8GHz ultra-low-power radar sensor, achieves exceptional efficiency by drawing only 30μA to 100μA of operating current, enabling continuous motion detection for years on a single AA battery depending on sensitivity and the selected detection distance.

This exceptional energy efficiency relies on smart sensing algorithm with proprietary multi-dimensional "Space and Time" sensing technology. This approach differs from traditional radar designs, which utilize high-performance DSP chips and extensive memory, resulting in inflated costs and high power consumption.

In June 2026, Kan was invited to France to attend the inaugural European Semiconductor FSNP Meetup. Held on June 4, 2026, at Château de Seguin near Bordeaux, this was an exclusive, invitation-only event for the semiconductor industry, co-hosted by the European chip R&D platform EuroCDP and Silicon Catalyst.EU. He presented this ultra-low-power microwave radar sensing technology based on time-and-space correlation algorithms. The technology's key strength lies in its integration of proprietary "Spatial Intelligence" and trajectory tracking, enabling it to accurately distinguish actual human movement from environmental noise in dynamic settings. It currently supports a sensing range of up to 20 meters and effectively prevents false triggers caused by natural wind, indoor fans, vibrations, or environmental noise.

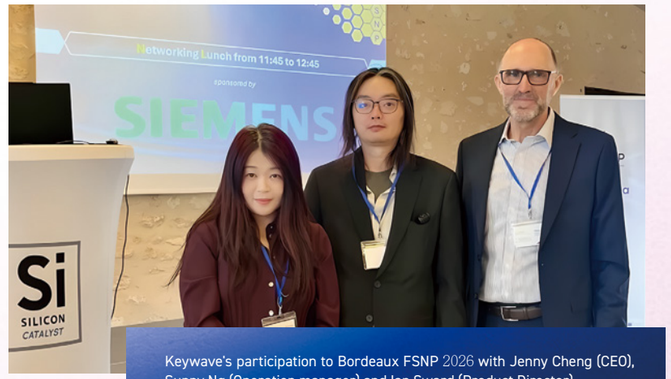
By combining radar sensors with AI technology, Keywave KW307, a 24GHz human presence and occupancy sensing module, enables the development of advanced, intelligent applications capable of detecting not only people and objects but even micro-motions like typing, breathing, or minor gestures. Given the regulatory restrictions in EU's General Data Protection Regulation (GDPR) and California's CCPA/CPRA regarding the major concerns of camera-based systems capturing real-person images or personal identifiers, Keywave's radar sensors have secured a significant market advantage by measuring motion, distance, and velocity.

These microwave radar sensors facilitate applications such as office occupancy monitoring, object trajectory analysis, and climate and lighting control, while integrating seamlessly with the Industrial IoT devices, robotics, and smart home sectors to rapidly expand the scope of smart use cases. Kan also revealed that the next-generation radar sensor currently under development aims to push detection boundaries from a few hundred meters to several kilometers. This will explore the business potentials for deeper integration with drone and robotics applications to assist autonomous systems with spatial awareness and reliable presence detection in variable or low-light conditions.

The most impressive technological breakthrough of Keywave Technology lies in its ability to achieve precise stationary presence detection and micro-motion tracking by analyzing the minute chest movements caused by breathing, even when a person is completely motionless. The current popular demonstration of Smart Spaces include powering privacy-compliant occupancy tracking for automated lighting and optimized HVAC adjustments. There are more use cases in the industrial controlling and detecting systems.

The company is currently actively forging partnerships across various sales channels, including IC distributors, ODM/OEM manufacturers, and system integrators. In addition to offering engineering evaluation kits, development boards and support to technical teams, Keywave is seeking strategic partners to collaborate closely on the co-design of new applications with hardware and software system integrators.

For further viewing the ultra-low-power radar porducts of Keywave, the company will exhibit at Microelectronics UK 2026, taking place at ExCeL London on September 29–30, 2026. The showcasing booth stand is located at Stand G16, ExCeL London, Royal Victoria Dock. At Keywave, we have been working on exciting new developments designed to help our partners navigate complex engineering challenges, optimize performance, and drive innovation. Visiting our booth will give you an exclusive look at our latest product demonstrations, upcoming technology roadmap, and a chance to speak directly with our technical experts.



Keywave's participation to Bordeaux FSNP 2026 with Jenny Cheng (CEO), Sunny Ng (Operation manager) and Ian Sward (Product Director)

Advanced process technology enters new phase as transistor architecture and materials innovation become key to extend Moore's law

DIGITIMES Intelligence, Derek Huang

Advanced semiconductor process technology has long relied on transistor miniaturization to improve chip performance, reduce power consumption, and optimize cost. However, as process nodes move below 2nm, the density gains from scaling alone have slowed markedly. Short-channel effects, leakage, and other physical limits are becoming more pronounced, pushing advanced process into a new phase characterized by higher cost, greater complexity, and slower gains.

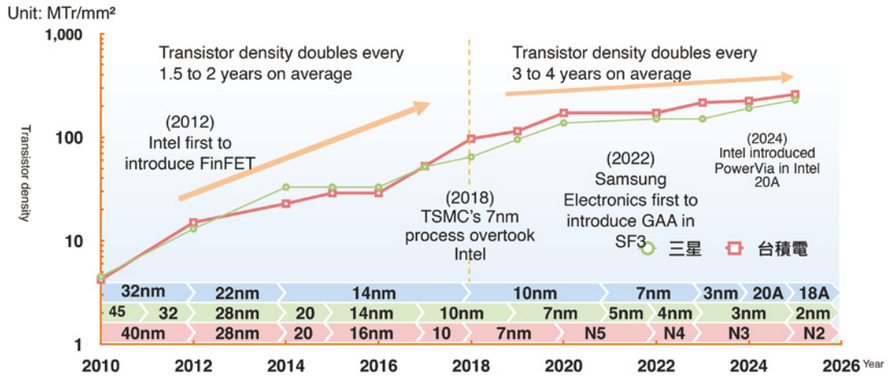
The focus of future advanced process development is no longer confined to miniaturization. It is shifting toward improvements in transistor architecture, back side power delivery, vertical stacking, and the introduction of non-silicon materials. TSMC, Intel, and Samsung are all currently moving toward gate-all-around field-effect transistor (GAA-FET) and backside power delivery technologies, but their technological trajectory and adoption timelines differ. The key competitive factor will be who can reliably bring highly complex new technologies into mass production while achieving the best balance between performance, cost, and yield.

Slower density gains put transistor architecture and backside power delivery at the center of continued scaling

DIGITIMES notes that over the past decade-plus, the semiconductor industry has mainly increased transistor density through process scaling, enabling chip designers to integrate more transistors in the same area and supporting the growth of smartphones, high-performance computing (HPC), and artificial intelligence (AI) chips. However, after the 7nm node, the marginal benefits of scaling have declined significantly.

Tighter component spacing has intensified issues such as current leakage, parasitic capacitance, contact resistance, and more. At the same time, advanced processes have become increasingly dependent on extreme ultraviolet (EUV) lithography equipment, while process control has become more difficult, and each node upgrade drives R&D and equipment investments significantly higher. As a result, alongside continued process scaling, transistor architecture innovation and back side power delivery have become important tools for sustaining density gains.

Transistor density and key process introductions at the three major foundries



In conventional chips, both power delivery and signal lines are placed on the front side of the wafer. As transistor density rises, however, routing space becomes increasingly constrained. Moving power delivery to the back side of the wafer not only allows the front side metal layers to focus on signal transmission, improving routing efficiency and logic density, but also helps improve power delivery efficiency and reduce power loss.

On back side power delivery, all three major manufacturers have established clear roadmaps, but timing and implementation choices differ. Intel is moving the fastest. It introduced the technology on Intel 18A and entered mass production in 2025. And the use of nano through-silicon vias (nTSVs) to deliver power from the back side of the wafer to the contact layer is seen as an important step in rebuilding market confidence in its advanced process technology.

TSMC plans to introduce the Super Power Rail (SPR) at the A16 node by the end of 2026. The approach connects the metal on the backside metal directly to the transistor contact layer, creating the shortest power delivery path and offering the greatest potential improvement in IR drop, while further optimizing logic density. Samsung is taking a more cautious approach to backside power delivery, prioritizing yield improvement in its 2nm process for now and planning to introduce the relevant technology at the SF2Z node in 2027. This strategy should help reduce the mass-production risks that come with introducing multiple new technologies at the same time.

Advanced process roadmap for TSMC, Intel, and Samsung Electronics

		2025		2026		2027	2028	2029		2030
TSMC	Nanosheet		N2	N2P	N2X	A16	A14	A13	A12	A10
	FinFET	N3P	N3X	N3A						
	EUV	0.33NA EUV								
Intel	RibbonFET	Intel 18A		Intel 18A-P			Intel 14A	Intel 14A-E		Intel 10A
	FinFET	Intel 3-T	Intel 3-E							
	EUV	0.33NA EUV					0.55NA EUV			
Samsung Electronics	MBCFET	SF3	SF2	SF2P	SF2X	SF2A	SF2Z	SF1.4		
	FinFET	SF4U								
	EUV	0.33NA EUV						0.55NA EUV		

Note: Backside power delivery processes are shown with a blue background

GAAFET takes over from FinFET as transistor architecture moves to the next generation

As channel dimensions approach their limits, GAAFET is becoming the mainstream architecture for the next phase of advanced process. Compared with FinFET, GAAFET's gate can wrap around the channel, providing stronger gate control, effectively reducing leakage, and improving short-channel effects.

In the transition between architectures, TSMC remains committed to a steady rollout strategy. It introduced the GAA structure in the N2 generation, then gradually strengthened performance and density through N2P, N2X, and A16. Its core advantages remain yield control, a large customer ecosystem, and a complete IP portfolio. Intel, by contrast, has adopted a more aggressive technical strategy, using GAAFET and backside power delivery as the two pillars of Intel 18A.

If it can achieve smooth mass production and gain adoption from key customers, Intel could increase its influence in the foundry market. Its biggest challenge is converting R&D results into a stable, cost-competitive volume-production platform. Samsung, meanwhile, was the first foundry to introduce GAAFET and tried to build an early-mover advantage through MBCFET. If it can gradually improve mass-production stability across the SF2 family and into SF1.4, Samsung still has an opportunity to expand its share in custom chips and mobile SoC markets.

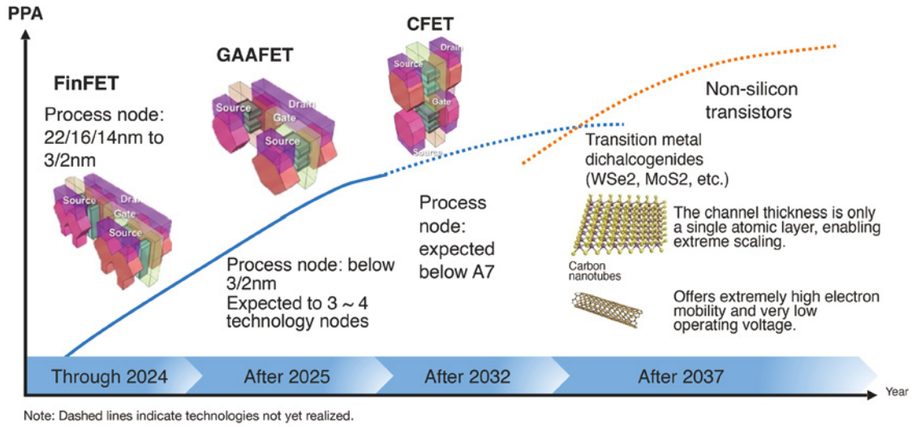
Complementary field-effect transistor (CFET) and non-silicon materials drive long-term vertical stacking and materials innovation

Although the GAA architecture can support several generations below 2nm, it will eventually face physical limits in the long term. To further increase density, advanced process will move from planar scaling to vertical integration, with CFET becoming an important next-generation direction.

The core idea of CFET is to vertically stack n-type and p-type transistors, significantly reducing standard cell area. However, vertical stacking places extremely high demands on process technology and introduces challenges in thermal management, contact resistance, and material epitaxy. As a result, CFET is expected to reach a level of production maturity for mass production only after 2030.

Looking further ahead, materials innovation will be key to breaking the limits of silicon-based semiconductors. As silicon channel thickness approaches its physical limit, non-silicon materials such as tungsten diselenide (WSe_2) and molybdenum disulfide (MoS_2), both transition metal dichalcogenides, are emerging as potential solutions. These two-dimensional materials can still maintain strong switching behavior at a monolayer thickness. However, the current semiconductor equipment base, electronic design automation (EDA) tools, and IP ecosystem are highly dependent on silicon platforms. For new materials to enter mass production, they must not only prove superior performance, but also clear commercialization hurdles in cost, yield, and large-area manufacturing.

Transistor form-factor changes and expected development in advanced processes



Note: Dashed lines indicate technologies not yet realized.

Conclusion: advanced processes have moved beyond simple line-width scaling; back side power delivery, vertical stacking, and new materials will continue to drive its development

The marginal gains from traditional scaling are gradually diminishing, and the industry is entering a new phase of competition with higher barriers. In the near to medium term, GAAFET and back side power delivery will support nodes below 2nm. In the medium to long term, CFET will drive vertical stacking. Further out, progress will depend on non-silicon materials such as two-dimensional materials to overcome physical limits.

TSMC, Intel, and Samsung are all actively investing in this broader competition. TSMC continues to introduce new technologies in a measured way; Intel is layering in multiple technologies at once to narrow the gap with competitors; and Samsung is pursuing an early GAAFET rollout and a gradual approach to back side power delivery. Ultimately, the foundry that best balances technology risk, yield control, customer adoption, and capital efficiency will be positioned to lead the next phase of advanced process.

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